HANDS-ON TECHNICAL TRAINING IN PHYSICAL DESIGN USING CADENCE EDA TOOL

Event No	EC035
Organizing Department	Electronics and Communication Engineering
Associate Dept. | NSC	International Society for Technology in Education
Date	03/11/2022 to 04/11/2022 (2 Days)
Time	09:00 AM to 05:00 PM
Event Type	VAC / Training Program
Event Level	Dept. Level
Venue	ECE Block - VLSI Lab
Total Participants	15
Faculty - Internal	6
Students - Internal	5
Other Participants	4

Related SDG

Resource Persons

Sl	Type	Name	Designation	Company	Email	Phone
1	Resource Person	Shivaprasad B K	Senior Field Application Engineer	Entuple Technologies Pvt. Ltd.	shivaprasad.bk@entuple.com	xxxxxxxxxx
2	Resource Person	Shivaprasad B K	Shivaprasad B K	Senior Field Application Engineer	shivaprasad.bk@entuple.com	xxxxxxxxxx

Involved Staffs

Sl	Name	Role
1	Muralidharan J	Coordinator
2	Ram Nivas D	Coordinator

Outcome

The participants can able to perform parameter estimation and analysis like Power estimation, Delay estimation, Floor planning and Area estimation in semi-custom mode as well as full-custom mode. Add on to that fault testing, fault detection and fault diagnosis also carried out.

Event Summary

The resource person is Mr. Shivaprasad B K, Senior Field Application Engineer, Entuple Technologies Pvt. Ltd. He has Completed M.Tech from B.V. Bhoomaraddi College of Engineering and Technology, Hubli, in 2014 (Affiliated to VTU, Belagavi) Specialization in VLSI Design and Testing and Completed Bachelor of Engineering from SJM Institute of Technology, Chitradurga, in 2012 (Affiliated to VTU, Belagavi) Specialization in Electronics and Communication Engineering department. He Worked as an Intern at ISRO Bangalore in the year 2014. Also he posses 8+ years of experience in the VLSI Design domain. He is also a Life time member of Indian Society for Technical Education(ISTE). The Department of Electronics and Communication Engineering, KPR Institute of Engineering and Technology organized a hands-on technical training program on Physical design using Cadence EDA Tool. ASIC design flow is a mature and silicon-proven IC design process which includes various steps like design conceptualization, chip optimization, logical/physical implementation, and design validation and verification. Physical design is process of transforming netlist into layout [GDSII]. Main steps in physical design are floorplanning, placement of all logical cells, clock tree synthesis & routing. During this process of physical design area, timing, power, design & technology constraints have to be met. Further design might require being optimized with respect to area, power, timing and performance. During the technical training various parameter estimation and analysis was done on combinational circuits among them few are Power estimation, Delay estimation, Floor planning and Area estimation in semi-custom mode as well as full-custom mode. Add on to that testing, detection and diagnosis of several faults also discussed.

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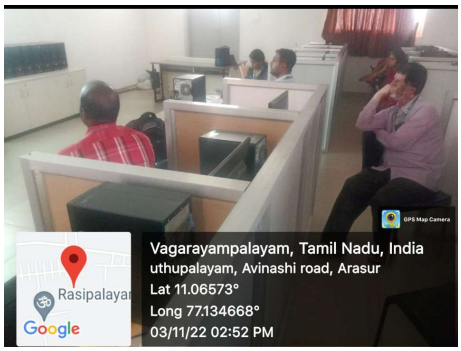

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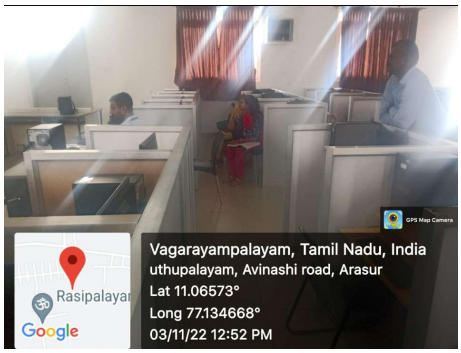

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